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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,484	04/08/2004	Michael G. Kelly	10031133-1	7400

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,484	KELLY, MICHAEL G.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. The appeal brief filed on 05/15/2006 on in response to the Office action mailed on 01/30/2006 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-21.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of Wu (2003/0067057).

4. Regarding claim 1, Hideshima (e.g. fig. 8) shows an integrated circuit system, comprising: a die 11 incorporating an integrated circuit and having a top side and a bottom side, the top side supporting an electrical signal communication metallization 15 b/e wherein the bottom side supporting a bottom side thermal dissipation metallization 16/43C but does not disclose a top side thermal dissipation metallization. Nevertheless, Wu (e.g. fig. 3A) shows a die a topside thermal dissipation metallization 21. This type of embodiment allows the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached

to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package (pp 0009). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a top side thermal dissipation metallization layer as disclosed by Wu to allow the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package as suggested by Wu.

5. Regarding claim 2, Hideshima shows that the electrical signal communication metallization comprises a plurality of exposed bonding elements on the top side of the die.

6. Regarding claim 3, Hideshima shows that the bonding elements are contained in a peripheral region of the topside of the die.

7. Regarding claim 4, Wu shows that the topside thermal dissipation metallization is disposed in a central region of the topside of the die.

8. Regarding claim 5, Wu shows that the topside thermal dissipation metallization is surrounded by the plurality of boning elements.

9. Regarding claim 6, White shows that the electrical signal communication metallization surrounds the top side thermal dissipation metallization.

10. Regarding claim 7, Hideshima shows that the topside thermal dissipation metallization comprises a patterned metal layer.

11. Regarding claim 8, Hideshima shows that the patterned metal layer comprises at least one through-hole.

12. Regarding claim 9, Hideshima shows that the patterned metal layer comprises an array of through-holes.

13. Regarding claim 21, Wu shows that the electrical signal communication metallization is free of any direct electrical connection to the top side thermal dissipation metallization on the top side of the die.

14. Claims 1-4 and 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of Kunikiyo (US 6,717,267).

15. Regarding claim 1, Hideshima shows an integrated circuit system, comprising: a die 11 incorporating an integrated circuit and having a top side and a bottom side, the top side supporting an electrical signal communication metallization 15 b/e wherein the bottom side supporting a bottom side thermal dissipation metallization 16/43C but does not disclose a top side thermal dissipation metallization. Nevertheless, Wu (e.g. fig. 3A) shows a die a topside thermal dissipation metallization 21. Nevertheless, Kunikiyo (e.g. fig. 19) shows a top side thermal dissipation metallization 31. According to Kunikiyo, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the interlayer insulating films. This improves the circuit operation of the semiconductor device (col. 23/lls. 1-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in Hideshima's invention a topside thermal dissipation metallization such as dummy patterns in accordance to

Kunikiyo's invention to improve the circuit operation since the heat can be satisfactorily removed form the interlayer insulating films.

16. Regarding claim 2, Hideshima shows that the electrical signal communication metallization comprises a plurality of exposed bonding elements on the top side of the die.

17. Regarding claim 3, Hideshima shows that the bonding elements are contained in a peripheral region of the topside of the die.

18. Regarding claim 4, Kunikiyo shows that the topside thermal dissipation metallization is disposed in a central region of the topside of the die..

19. Regarding claim 6, Kunikiyo shows that the electrical signal communication metallization surrounds the topside thermal dissipation metallization (e.g. plugs).

20. Regarding claim 7, Kunikiyo shows that the topside thermal dissipation metallization comprises a patterned metal layer.

21. Regarding claim 8, Hideshima shows that the patterned metal layer comprises at least one through-hole.

22. Regarding claim 9, Hideshima shows that the patterned metal layer comprises an array of through-holes.

23. Regarding claim 10, Kunikiyo shows a top heat spreader 32 metallurgically bonded to the op side thermal dissipation metallization of the die.

24. Regarding claim 11, Kunikiyo shows that the integrated circuit is connected electrically to the op side heat spreader by an electrical path extending through the top side thermal dissipation metallization.

25. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of Kunikiyo (US 6,717,267) further in view of Wang (US 5,977,626).

26. Regarding claim 12, Hideshima in view of Kunikiyo shows most aspects of the instant invention except for an electrical interface and a substrate containing a wiring interconnection between the electrical signal communication metallization and the electrical interface. Nevertheless, Wang (e.g. fig. 4) shows a package having a good efficiency of spreading heat and enhanced EM shielding that includes an electrical interface 28 and a substrate 20 containing a wiring interconnection between the electrical signal communication metallization and the electrical interface (col. 1/lls. 11-33; col. 2/lls. 10-14 & col. 3/lls. 10-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the package disclosed by Wang to package the device disclosed by Hideshima in view Kunikiyo, which includes an electrical interface and a substrate containing a wiring interconnection between the electrical signal communication metallization and the electrical interface, because this package structure has a good efficiency of spreading heat and enhanced EM shielding as taught by Wang.

27. Regarding claim 13, Wang shows a top heat spreader 32 mounted on the substrate and forms a lid of the package covering the topside of the die.

28. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of Kunikiyo (US 6,717,267) further in view of Khan et al. (US 6,853,070).

29. Regarding claim 14, Hideshima in view of Kuńikiyo shows most aspects of the instant invention but does not disclose a structure having a second heat spreader or bottom heat spreader metallurgically bonded to the bottom side thermal dissipation metallization of the die. Nevertheless, Khan (e.g. fig. 2A) shows a bottom heat spreader 110 ́bonded to the bottom side thermal dissipation metallization of the die 102. According to Kahn this type of mounting structure provides an improved thermal, mechanical and electrical performance because the thermal stress is reduced due to a matched thermal coefficient (col. 1/lls. 52-67; col. 2/lls. 1-6 and col. 3/lls. 14-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to metallurgically bond a bottom heat spreader to the bottom side thermal dissipation metallization of the die disclosed by Hideshima view of Kunikiyo to improve the thermal, mechanical and electrical performance of the package as taught by Khan.

30. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of White (US 5,665,655) further in view of Kunikiyo (US 6,717,267).

31. Regarding claim 15, Hideshima (e.g. fig. 8) shows most aspects of the instant invention including a method of making an integrated circuit system including the steps of: forming a integrated circuit dice 11 having a top supporting wherein the top supporting exposes electrical signal communication metallization 15/b/e; forming on a bottom side of the dice having a bottom side thermal dissipation metallization 16/45C; but does not include the step of forming multiple die regions on a substrate, forming a top side thermal dissipation metallization and the step of singulating the die regions to

form the integrated circuit dices. Nevertheless, White (e.g. figs. 5-8) shows a method including the step of forming multiple die regions on a substrate and the step of he step of singulating the die regions to form the integrated circuit dices. This method increases the yield of devices per wafer because microcrack propagation is reduced (col. 1/lls. 50-55; col. 2/lls. 10-12 & 45-51). Kunikiyo (e.g. fig. 19) shows the step of forming a topside thermal dissipation metallization 31. According to Kunikiyo, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the interlayer insulating films. This improves the circuit operation of the semiconductor device (col. 23/lls. 1-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hideshima's method in accordance to White's teachings which include the step forming multiple die regions on a substrate and the step of the step of singulating the die regions to form the integrated circuit dices to increase the yield of devices per wafer since microcrack propagations can be reduced and to include the step of forming a topside thermal dissipation metallization such as dummy patterns in the method disclosed by Hideshima in view of White to improve the circuit operation because the heat can be satisfactorily removed form the interlayer insulating films as taught by Kunikiyo.

32. Regarding claim 16, Hideshima in view of White further in view of teaches that in each die region, the electrical signal communication metallization surrounds the topside thermal dissipation metallization.

33. Regarding claim 17, Kunikiyo teaches that each topside thermal dissipation metallization comprises an exposed metal layer with an array of through-holes (e.g. 26a).

34. Regarding claim 18, Kunikiyo (e.g. fig. 19) shows the step of metallurgically bonding a top heat spreader of the package 32 (e.g. 31) to the topside thermal dissipation metallization of the singulated die (dummy pattern 25a).

35. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Hideshima et al. (US 5,143,865) in view of White (US 5,665,655) further in view of Kunikiyo (US 6,717,267) further in view of Wang (US 5,977,626).

36. Regarding claim 19, Hideshima in view of White further in view of Kunikiyo shows most aspects of the instant invention but does not show that the package including a substrate a mounting step comprising the step of mounting the package substrate to the bottom side thermal dissipation metallization of the singulated die. Nevertheless, Wang (e.g. fig. 4) shows a method including a substrate 20 and the step of mounting the bottom side a singulated die 22 to the substrate. This package provides a good efficiency of spreading heat and enhanced EM shielding (col. 1/lls. 11-33; col. 2/lls. 10-14 & col. 3/lls. 10-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method disclosed by Wang to package the device disclosed by Hideshima in view of White further in view Kunikiyo, which includes the step of mounting the bottom side a singulated die to the substrate, because this method produce a package structure having a good efficiency of spreading heat and an enhanced EM shielding as taught by Wang.

Response to Arguments

37. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

39. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

40. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leonardo Andújar
Primary Examiner
Art Unit 2826